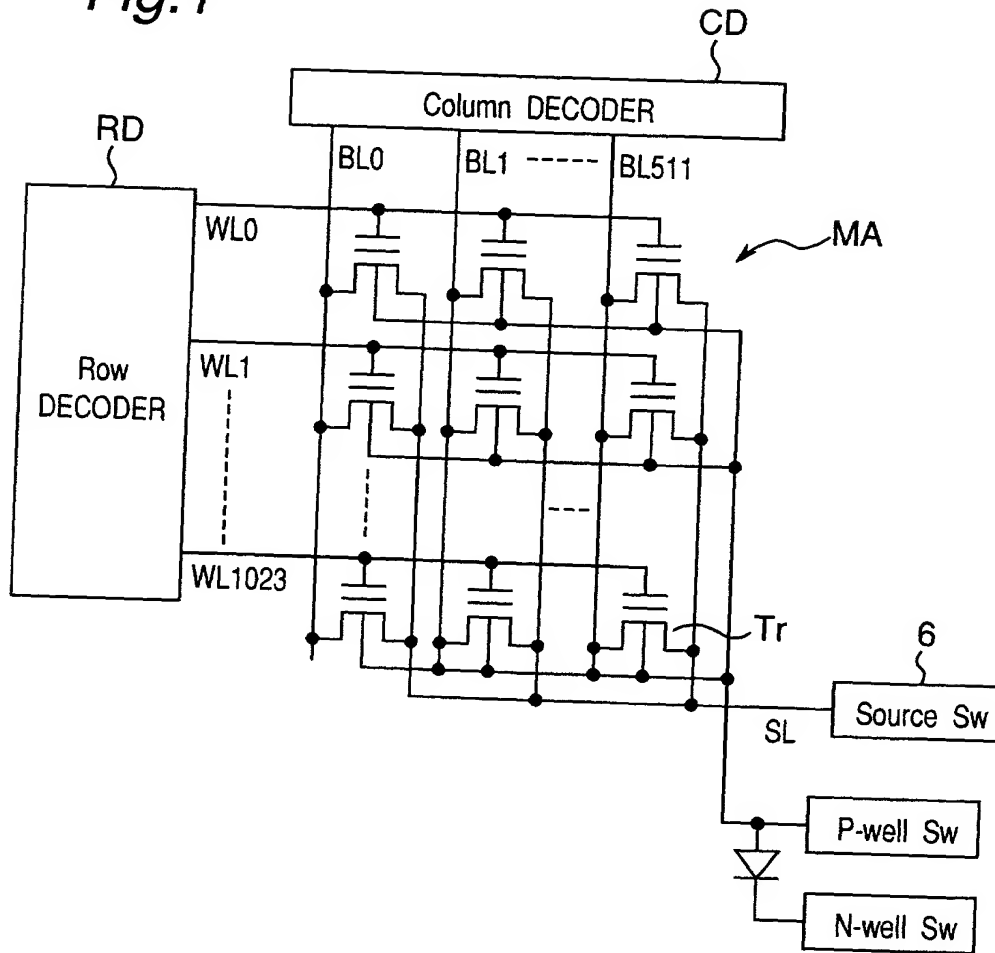


Fig. 1



The diagram illustrates a semiconductor device structure and its electrical connections. The main component is a memory array (10) consisting of a substrate with P-well (11) and N-well (12) regions. A word line (WL) is connected to access transistors (Tr) and storage capacitors (15, 16, 17, 18). The device is connected to various pumping circuits (1, 2, 3) and switches (4, 5) for high-voltage and negative voltage control.

- 1**: FIRST HIGH-VOLTAGE PUMPING CIRCUIT
- 2**: SECOND HIGH-VOLTAGE PUMPING CIRCUIT
- 3**: NEGATIVE VOLTAGE PUMPING CIRCUIT
- 4**: P-Well Sw
- 5**: N-Well Sw
- RD**: Row Decoder
- WL**: Word Line
- Tr**: Access Transistor
- 11**: P-well
- 12**: N-well
- 15**: Storage Capacitor
- 16**: Storage Capacitor
- 17**: Storage Capacitor
- 18**: Storage Capacitor

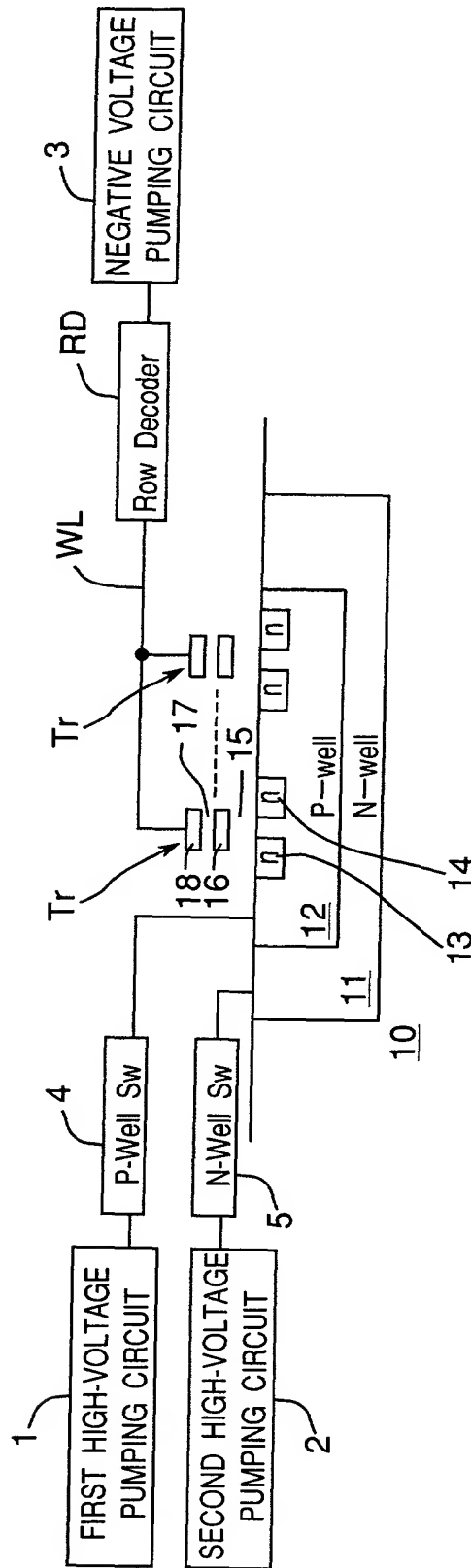


Fig.3

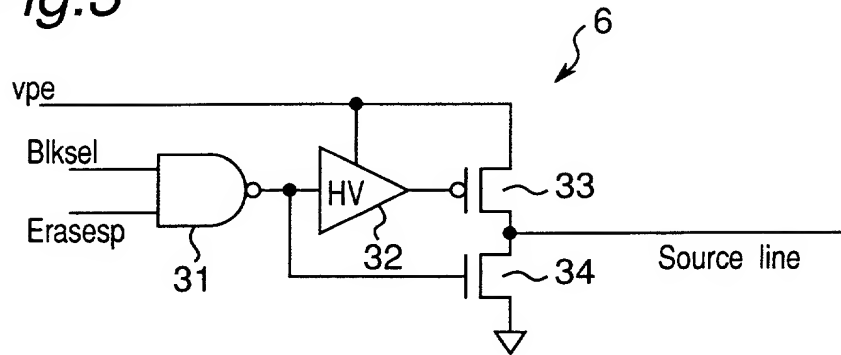


Fig.4

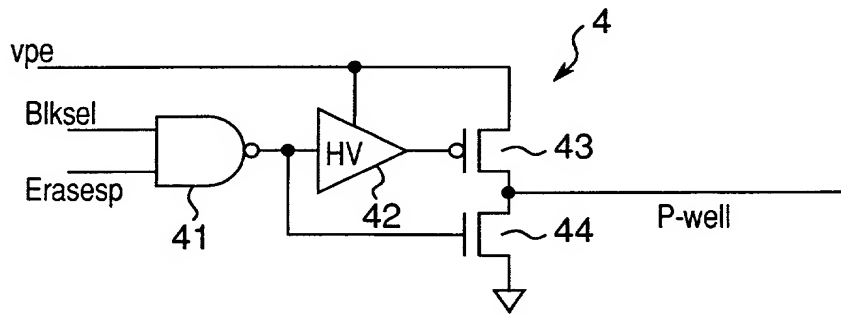


Fig.5

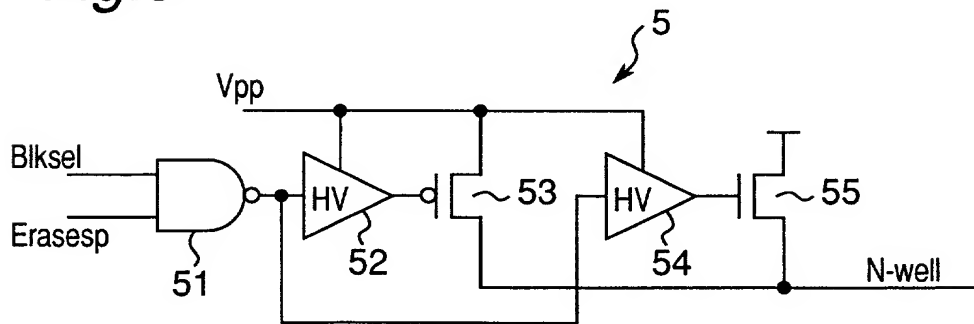


Fig.6

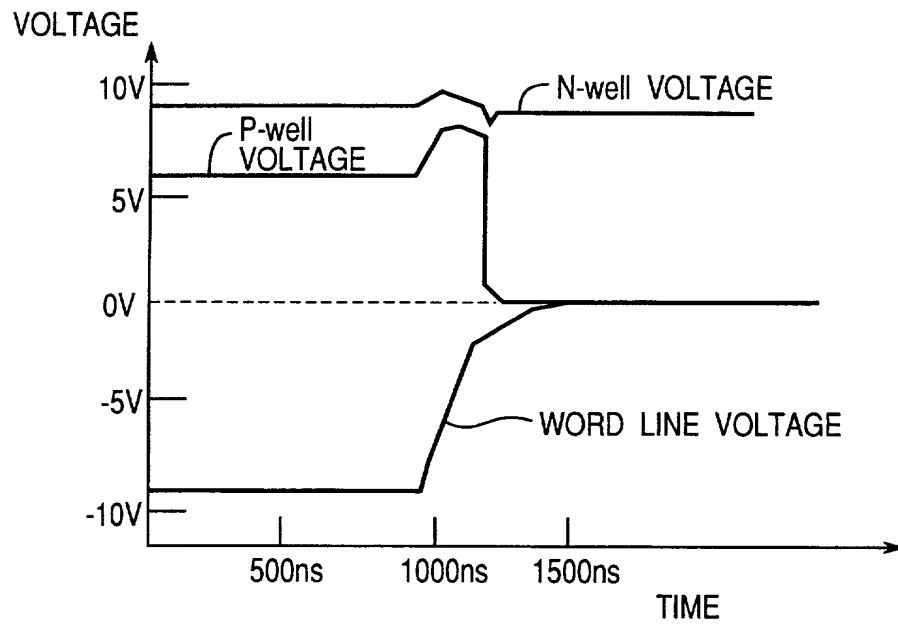


Fig. 7

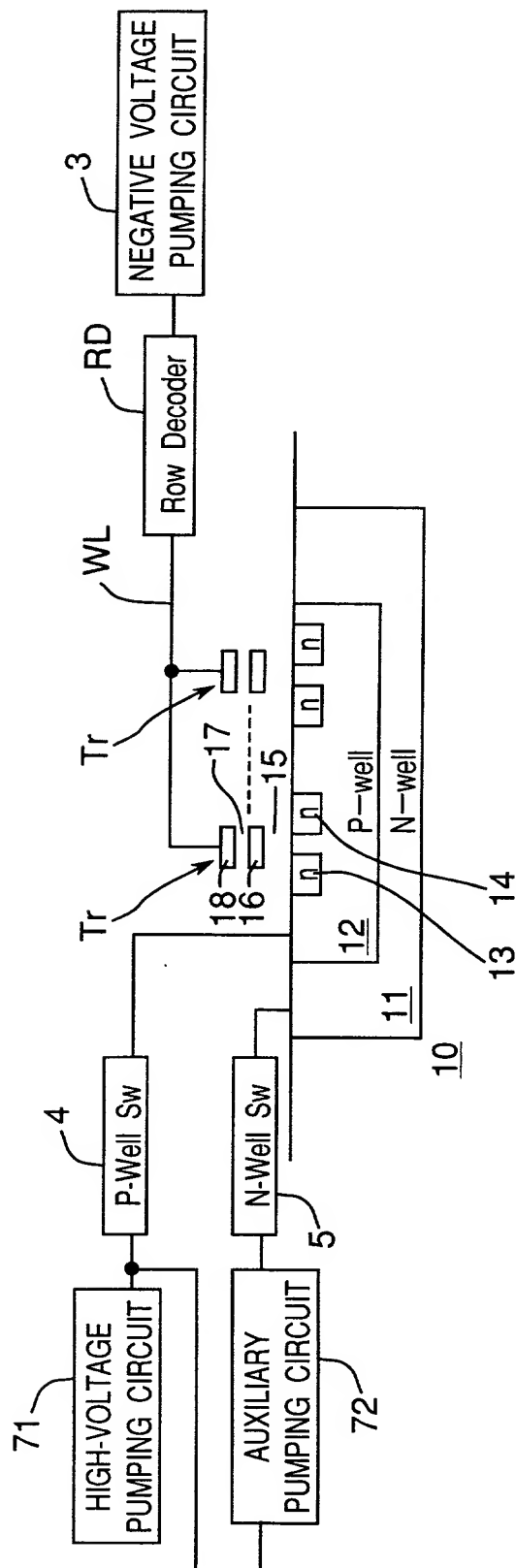


Fig.8

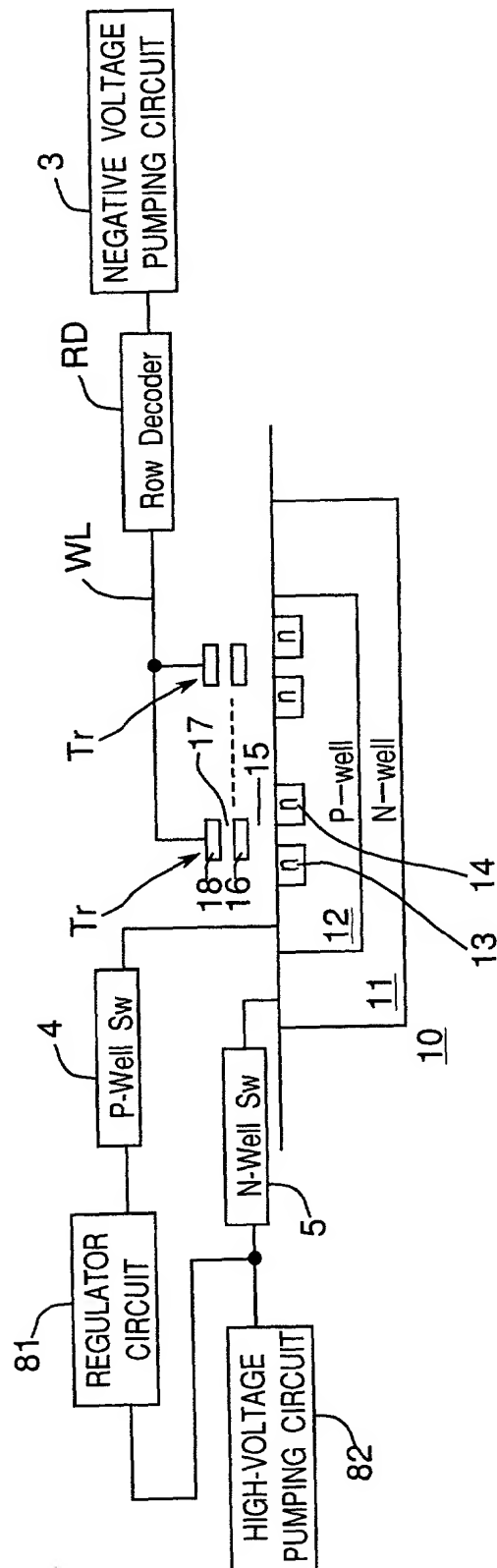


Fig.9

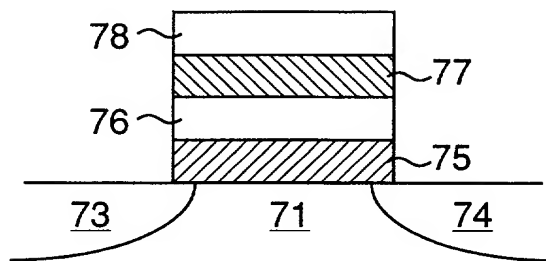


Fig.10

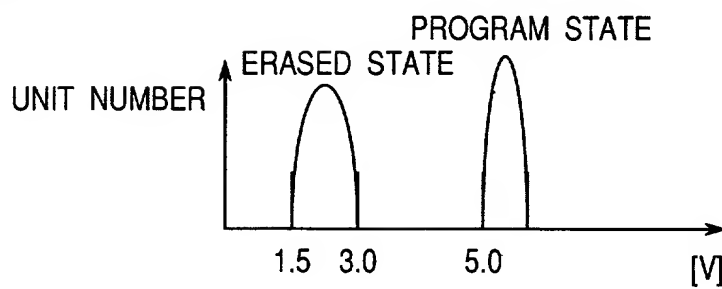


Fig.11

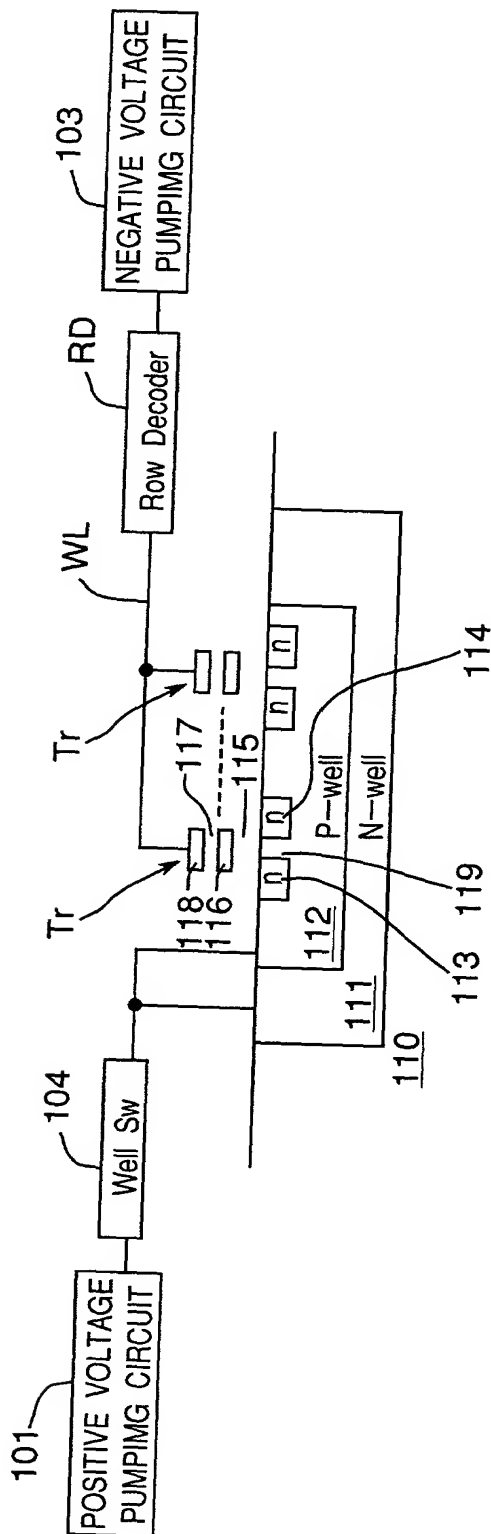


Fig. 12

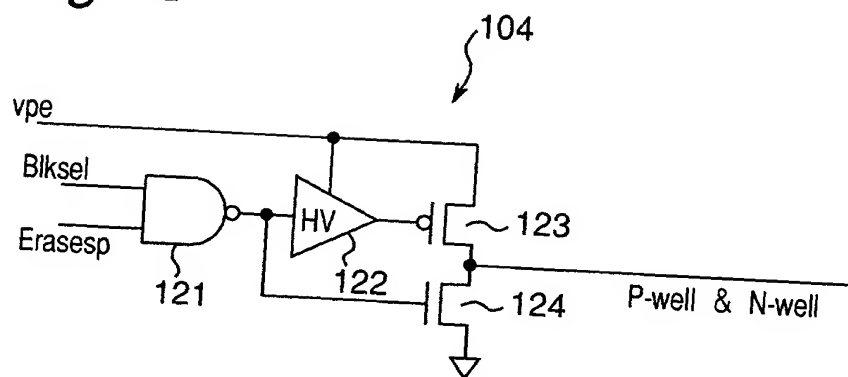


Fig.13

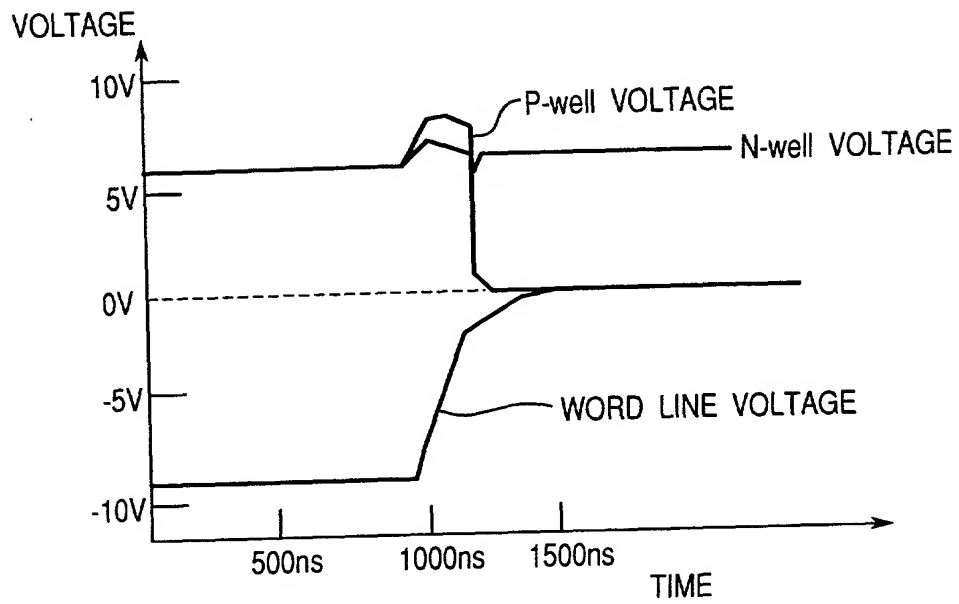


Fig.14

